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**What is claimed is:**

1. A clock compensation circuit, comprising:
  - a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;
  - a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals; and
  - a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.
2. The clock compensation circuit of claim 1, wherein the clock synchronization circuit comprises:
  - a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and
  - a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.
3. The clock compensation circuit of claim 1, wherein the one of the plurality of internal logic clock signals is matched in frequency to the sample clock.
4. The clock compensation circuit of claim 1, wherein the synchronization circuit receives an input clock signal on the order of 100 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz.
5. The clock compensation circuit of claim 1, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

6. The clock compensation circuit of claim 1, wherein the down converter channel produces two selectable outputs that are 180 degrees out of phase.
7. A digital down converter, comprising:
  - a clock compensation circuit including:
    - a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;
    - a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals; and
    - a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.
8. The digital down converter of claim 7, wherein the clock synchronization circuit comprises:
  - a phase-locked loop coupled to receive the input clock signal and to generate the

master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

9. The digital down converter of claim 7, wherein the one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

10. The digital down converter of claim 7, wherein the synchronization circuit receives an input clock signal on the order of 100 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz.

11. The digital down converter of claim 7, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

12. A clock compensation circuit, comprising:

an input for receiving an input clock signal;

a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a tapped delay line coupled to receive a first one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal;

a phase comparator coupled to receive a second one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the sample clock; and

a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal.

13. The clock compensation circuit of claim 12, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

14. The clock compensation circuit of claim 12, wherein the clock divider receives a master clock signal on the order of 200 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz.

15. The clock compensation circuit of claim 12, wherein the second one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

16. The clock compensation circuit of claim 12, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the second one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the second one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

17. A clock compensation circuit, comprising:

an input for receiving an input clock signal;

a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a phase comparator coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals;

a tapped delay line coupled to receive a second one of the plurality of internal logic clock signals and to generate a delayed clock signal for input to the associated receiver, wherein the delayed clock signal is synchronized with the sample clock; and

a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signal.

18. The clock compensation circuit of claim 17, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

19. The clock compensation circuit of claim 17, wherein the first one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

20. The clock compensation circuit of claim 17, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

21. A communications system, comprising:

a plurality of receivers, wherein each receiver is coupled to receive a data signal and a clock signal;

a digital down conversion circuit, including:

a clock synchronization circuit coupled to receive an input clock signal,  
wherein the clock synchronization circuit generates a master clock  
signal and produces a plurality of internal logic clock signals;

a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock signal from an associated one of the plurality of receivers and to generate a control signal based on a comparison of the phase of the first one of the plurality of internal logic clock signals with the sample clock signal; and

a plurality of down converter channels, wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals and the control signal and passes data from the data signal in phase with the sample clock signal.

22. The communications system of claim 21, wherein the synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal therefrom; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals therefrom.

23. The communications system of claim 21, wherein each of the down converter channels comprises:

a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed is in phase with the sample clock signal.

24. The communications system of claim 21, further comprising a tapped delay line coupled to receive a second one of the plurality of internal logic clock signals and to generate a plurality of output clock signals with a selected delay based on the second one of the plurality of internal logic clock signals, wherein each of the plurality of output clock signals is used by the associated receiver to generate the sample clock.



when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge of the one of the plurality of internal logic clock signals; and  
passing the selected data signal to the associated receiver.

27. A communications system, comprising:  
a plurality of analog to digital converters;  
a digital down converter coupled to receive an input clock signal from one of the plurality of analog to digital converters, wherein the digital down converter includes:  
a clock synchronization circuit coupled to receive the input clock signal and to generate a master clock signal and a plurality of internal logic clock signals;  
a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver, and wherein each phase comparator generates a control signal based on a phase comparison between the sample clock and the first one of the plurality of internal logic clock signals;  
a plurality of down converter channels, wherein each down converter channel is coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signal;  
a plurality of receivers, each receiver associated with one of the plurality of phase comparators and one of the plurality of down converter channels; and  
a tapped delay line coupled to a second one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal for each of the plurality of receivers.

28. The system of claim 27, wherein each of the plurality of down converter channels comprises:  
a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed is in phase with the sample clock signal.

29. The system of claim 27, wherein each of the clock synchronization circuits comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

30. A clock compensation circuit, comprising:

a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates at least one internal logic clock signal;

a phase comparator coupled to receive the at least one internal logic clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the at least one internal logic clock signal; and

a down converter channel coupled to receive the at least one internal logic clock signal and the control signal and to pass data in phase with the sample clock using the internal logic clock signal based on the control signal.

31. A clock compensation circuit, comprising:

a phase comparator coupled to receive a first clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the first clock signal; and

